

WHAT IS CLAIMED:

- 1 1. An integrated circuit, comprising:
2 functional circuitry;
3 a region devoid of the functional circuitry; and
4 a transistor disposed in the region.
- 1 2. The integrated circuit of claim 1 wherein:
2 the functional circuitry comprises functional-circuit blocks that are spaced
3 apart from one another; and
4 the devoid region comprises a region that is disposed between the
5 functional-circuit blocks.
- 1 3. The integrated circuit of claim 1 wherein:
2 the functional circuitry comprises a functional-circuit block having a portion
3 devoid of functional-circuit elements; and
4 the devoid region comprises the devoid portion of the functional-circuit block.
- 1 4. The integrated circuit of claim 1 wherein the transistor comprises an FET
2 transistor.
- 1 5. The integrated circuit of claim 1 wherein the transistor is automatically
2 placed in the devoid region.
- 1 6. The integrated circuit of claim 1 wherein the transistor is manually placed in
2 the devoid region.
- 1 7. An integrated circuit, comprising:
2 functional circuitry;
3 a region devoid of the functional circuitry; and
4 a buffer disposed in the region.
- 1 8. An integrated circuit, comprising:
2 functional circuitry;
3 a region devoid of the functional circuitry; and
4 a logic circuit disposed in the region.

1 9. The integrated circuit of claim 8 wherein the logic circuit comprises a logic
2 gate.

1 10. The integrated circuit of claim 8 wherein the logic circuit comprises an
2 inverter.

1 11. An integrated circuit, comprising:
2 first and second supply nodes;
3 functional circuitry;
4 a region devoid of the functional circuitry; and
5 a transistor disposed in the region and having a pair of input-output terminals
6 coupled to the first supply node and having a control terminal coupled
7 to the second supply node.

1 12. The integrated circuit of claim 11 wherein:
2 the transistor comprises an FET transistor;
3 the pair of input-output terminals comprises a pair of source-drain terminals;
4 and
5 the control terminal comprises a gate terminal.

1 13. An integrated circuit, comprising:
2 a conductive path;
3 functional circuitry;
4 a region devoid of the functional circuitry; and
5 a transistor disposed in the region and having a pair of input-output terminals
6 coupled to the conductive path and having a control terminal.

1 14. The integrated circuit of claim 13, further comprising:
2 a supply node; and
3 wherein the control terminal is coupled to the supply node.

1 15. The integrated circuit of claim 13 wherein the control terminal is coupled
2 to one of the input-output terminals.

1 16. The integrated circuit of claim 13 wherein the control terminal is
2 short-circuited to one of the input-output terminals.

1 17. An integrated circuit, comprising:
2 first and second regions;
3 functional circuitry disposed in the first and second regions;
4 a third region devoid of the functional circuitry;
5 a buffer disposed in the third region and having an input terminal and an
6 output terminal;
7 a first conductive path having a first terminal coupled to the functional circuitry
8 in the first region and having a second terminal coupled to the input
9 terminal of the buffer; and
10 a second conductive path having a first terminal coupled to the output terminal
11 of the buffer and having a second terminal coupled to the functional
12 circuitry in the second location.

1 18. The integrated circuit of claim 17 wherein the functional circuitry in the first
2 and second regions respectively comprises first and second blocks of the functional
3 circuitry, the first and second blocks being spaced apart from one another.

1 19. The integrated circuit of claim 17, further comprising:
2 a supply node; and
3 wherein the buffer comprises a transistor disposed in the devoid region and
4 having a control terminal coupled to the input terminal of the buffer, a
5 first terminal coupled to the output terminal of the buffer, and a second
6 terminal coupled to the supply node.

1 20. An integrated circuit, comprising:
2 first and second regions;
3 functional circuitry disposed in the first and second regions;
4 a third region devoid of the functional circuitry;
5 a logic circuit disposed in the third region and having an input terminal and an
6 output terminal;
7 a first conductive path having a first terminal coupled to the functional circuitry
8 in the first region and having a second terminal coupled to the input
9 terminal of the logic circuit; and

10 a second conductive path having a first terminal coupled to the output terminal
11 of the logic circuit and having a second terminal coupled to the
12 functional circuitry in the second location.

1 21. An integrated circuit, comprising:
2 functional circuitry;
3 a region devoid of the functional circuitry; and
4 a repair transistor disposed in the region and having a three terminals, one of
5 the terminals coupled to the functional circuitry.

1 22. The integrated circuit of claim 21 wherein two of the transistor terminals
2 are coupled to the functional circuitry.

1 23. The integrated circuit of claim 21 wherein the three transistor terminals
2 are coupled to the functional circuitry.

1 24. A method, comprising:
2 identifying an integrated-circuit region that is devoid of a circuit; and
3 placing a transistor in the devoid integrated-circuit region.

1 25. The method of claim 24 wherein identifying the devoid integrated-circuit
2 region and placing the transistor comprise executing software that identifies and
3 places the transistor in the devoid integrated-circuit region.

1 26. The method of claim 24 wherein placing the transistor comprises
2 executing software that automatically places the transistor in the devoid
3 integrated-circuit region.

1 27. The method of claim 24 wherein placing the transistor comprises
2 executing software that allows one to manually place the transistor in the devoid
3 integrated-circuit region.

1 28. The method of claim 24, further comprising connecting the transistor to
2 a supply node.

1 29. The method of claim 24, further comprising:
2 identifying a conductive path; and
3 connecting the transistor to the path.

1 30. The method of claim 24, further comprising:
2 identifying a conductive path; and
3 buffering the path with the transistor.

1 31. The method of claim 24 wherein placing the transistor comprises placing a
2 logic circuit in the devoid integrated-circuit region.

1 32. A method, comprising:
2 forming a circuit in a first region of an integrated circuit; and
3 forming a transistor in a second region of the integrated circuit, the second region
4 being devoid of the circuit.

1 33. The method of claim 32, further comprising:
2 forming first and second supply nodes;
3 coupling a first terminal of the transistor to the first supply node; and
4 coupling second and third terminals of the transistor to the second supply node.

1 34. The method of claim 32, further comprising:
2 forming a conductive path; and
3 coupling first, second, and third terminals of the transistor to the conductive path.

1 35. The method of claim 32, further comprising:
2 forming a supply node;
3 forming a conductive path;
4 coupling first and second terminals of the transistor to the conductive path; and
5 coupling a third terminal of the transistor to the supply node.

1 36. The method of claim 32, further comprising:
2 forming first and second segments of a conductive path;
3 coupling an input terminal of the transistor to the first segment; and
4 coupling an output terminal of the transistor to the second segment.

1 37. The method of claim 32, further comprising:
2 forming first and second segments of a conductive path that is coupled to the circuit;
3 coupling an input terminal of the transistor to the first segment; and
4 coupling an output terminal of the transistor to the second segment.

1 38. The method of claim 32, further comprising coupling the transistor to
2 the circuit to repair a defect in the circuit.

1 39. The method of claim 32, further comprising:
2 forming a conductive path;
3 dividing the conductive path into first and second uncoupled segments; and
4 coupling the first segment to the second segment with the transistor.

1 40. A method, comprising;
2 dividing an array into locations, the array representing an integrated-circuit;
3 identifying the locations in the array unoccupied by circuit blocks; and
4 placing transistors in the unoccupied locations.

1 41. The method of claim 40 wherein placing transistors comprises placing
2 blocks of transistors in the unoccupied locations.

1 42. A method of integrating additional transistors into an integrated circuit,
2 the method comprising:
3 calculating the dimensions of an array to store validity data;
4 initializing the array as valid;
5 reading block information including location and dimensions;
6 calculating the locations in the validity array corresponding to the block location and
7 dimensions;
8 marking the locations in the validity array as invalid;
9 checking for more blocks;
10 if more blocks are found, looping back to the step of reading block information;
11 if no more blocks are found, continuing:
12 for each location in the validity array, if valid, then place a transistor array block;
13 else, continue to next location.

1 43. The method of claim 42, further comprising allowing a user to invalidate
2 locations within the validity array.